Rajath V

Bengaluru , KA - IND

rajath.v.05@gmail.com +91 6364691230 linkedin.com/in.rajathv5

Work Experience

- **Nexthop AI** Bengaluru, KA, IND
  Software Engineer *Jan 2025 - Present*
  - **SONiC OS Platform Development**:
    - Working on **SONiC OS** platform development, focusing on config management, CLI enhancements, **Yang modeling**, and **Dynamic Load Balancing** feature implementation.
    - Developed an internal **Slack notification service** for distributed test engine runs, enabling per-user test schedule tracking with real-time updates.
    - Designed database schema with **in-memory caching** for performance optimization and implemented **data retention policies** with automated cron jobs for storage management.
- **Cisco Systems - Data Center AI Networking** Bengaluru, KA, IND
  Software Engineer II *Aug 2023 - Dec 2024*
  - **Layer 2 Feature Manager / VxLAN**:
    - Designed and developed **Ethernet Segment Identifier (ESI)** feature integrations with 2-way and 4-way multi-homing into packet forwarding components.
    - Contributed to **Broadcom ASIC SDK upgrade** by triaging and fixing post-upgrade defects across L2 components.
    - Built an **AI agent-based MCP server** for accelerated debugging of configurations on local development testbeds, improving feature development velocity.
    - Implemented end-to-end data ingestion pipeline using **ELK stack and Kafka** for multi-service log visualization and discrepancy detection.
    - Designed and developed a dashboard to enable debugging insights for Developer UT setups, integrating **pyATS testing** with topology loads.
    - Conceptualized and implemented a new schema in **Python** to output Hardware-Software consistency checks for Storm Control to fast-track debugging.
    - Architected higher-scale Layer 2 mac-learning template with stakeholder buy-in, achieving **2x scale improvements** in MAC address learning capacity.
    - Developed a service to maintain binary records of MAC address event histories in hardware drivers using **low-priority threads** for scale handling.
    - Achieved **20% improvement** in mac-learn rates (20 seconds at scale) and **50% optimization** in out-of-memory log collection (1M+ lines optimized).
- **Cisco Systems - Data Center Switching** Bengaluru, KA, IND
  Software Engineering Intern *May - Jul 2022 & Jan - Jun 2023*
  - **Layer 2 Feature Manager**:
    - Migrated tech-support components from single-threaded to **multi-threaded architecture**, reducing execution and log-collection time by **50%**.
    - Designed and developed an internal tool to clean up event-based logs by sorting based on timestamps and grouping by VLANs.

Projects

- **Gait Analysis**:
  - Design Project under Prof. Tanmay Verlekar, BITS Pilani Goa. Developed a deep-learning model using **OpenPose** to classify gait sequences into five categories, achieving **89% accuracy** for preliminary gait deformity identification.
- **Speech Programmer**:
  - Open-source contributor to text-to-C-code web application. Implemented complex parsing for TextToSpeech output commands (functions, loops, variables) — an exercise in **accessibility awareness** in the open-source community.

Skills

- **Technologies**: SONiC OS, Distributed Systems, VxLAN Architecture, Packet Forwarding, Yang Modeling
- **Tools**: Kafka, ElasticSearch, Logstash, Kibana, Postgres, Linux, Git, pyATS
- **Languages**: C, C++, Python, Shell Scripting, LaTeX

Education

- **BITS Pilani** Sancoale, Goa, IND
  Bachelor of Engineering in Computer Science; CGPA: 8.71/10 *Aug. 2019 – Jun. 2023*